

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

- 1 1. (Currently amended): A method for manufacturing a semiconductor
2 power device, comprising:
3 identifying an active region on a semiconductor die, the active region having a
4 central portion, ~~and~~ a first peripheral portion disposed about a periphery of said central portion,
5 and a second peripheral portion disposed about a peripheral region of said first peripheral
6 portion;
7 identifying a first region in said central portion of said active region;
8 identifying a second region in said first peripheral portion of said active region;
9 identifying a third region in said second peripheral portion;
10 fabricating active cells in accordance with a first cell design in said first region;
11 fabricating active cells in accordance with a second cell design in said second
12 region, wherein ~~a combined~~ an operational current density of said active cells fabricated
13 according to said second cell design is greater than ~~a combined current density that~~ of said active
14 cells fabricated according to said first cell design ~~during operation of said active cells. , and~~
15 fabricating active cells in accordance with a third cell design in said third region,
16 wherein the operational current density of said active cells fabricated according to said third cell
17 design is greater than that of said active cells fabricated according to said second cell design.
- 1 2. (Original): The method of claim 1 wherein said first cell design and said
2 second cell design include cell dimensions such that a cell density of said first region is different
3 from that of said second region.
- 1 3. (Original): The method of claim 1 wherein said first cell design includes
2 at least one physical dimension different from that included in said second cell design.

1 4. (Original): The method of claim 3 wherein said physical dimension
2 includes a channel width.

1 5. (Original): The method of claim 4 wherein said physical dimension
2 includes a cell die area.

1 6. (Original): The method of claim 1 wherein said first cell design includes a
2 material composition for cells that is different from that of said second cell design.

1 7. (Currently amended): The method of claim 1 wherein said first cell design
2 differs from said second cell design with respect to ~~current density~~ cell density.

1 8. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to source resistance.

1 9. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to transconductance.

1 10. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to gain.

1 11. (Original): The method of claim 1 wherein said first cell design differs
2 from said second cell design with respect to threshold voltage.

1 12. (Original): The method of claim 1 wherein said first cell design and said
2 second cell design are field effect transistors.

1 13. (Original): The method of claim 1 wherein said first cell design and said
2 second cell design are memory cells.

1 14. (Previously presented): A semiconductor power device fabricated in
2 accordance with the method of claim 1.

1 15. (Currently amended): The method of claim 1 ~~further comprising~~
2 ~~disposing a plurality of terminating cells about a periphery of said active region~~ wherein said
3 first cell design differs from said second cell design with respect to pitch of gate stripes of each
4 cell design.

16. (Canceled).

1 17. (Currently amended): A method for manufacturing a semiconductor
2 power device, comprising:
3 identifying an active region on a semiconductor die;
4 identifying a first region in said active region;
5 identifying a second region in said active region;
6 identifying a third region in said active region;
7 providing a first cell design by which active cells in said first region will be
8 fabricated;
9 providing a second cell design by which active cells in said second region will be
10 fabricated; and
11 providing a third cell design by which active cells in said third region will be
12 fabricated,
13 wherein an operational current density of first second active cells fabricated
14 according to said ~~first second~~ cell design is greater than that of ~~are different from second first~~
15 active cells fabricated according to said ~~second first~~ cell design,
16 wherein the operational current density of third active cells fabricated according
17 to said third cell design ~~are different from~~ is greater than that of ~~said first active cells and from~~
18 said second active cells under the same biasing condition.
19 ~~wherein said first cell design and said second cell design are memory cells.~~